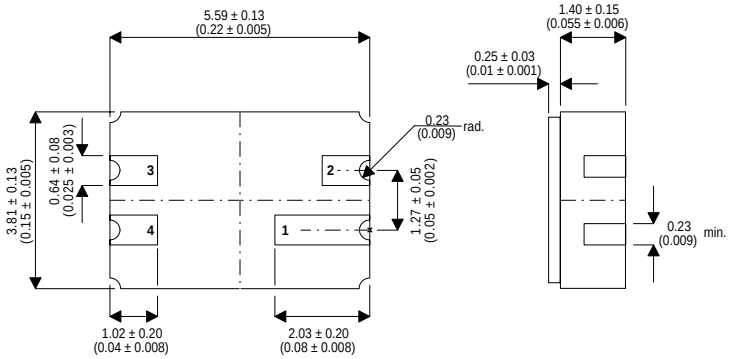
SML2955CSM4

P–CHANNEL ENHANCEMENT MODE MOSFET

MECHANICAL DATA
Dimensions in mm (inches)



LCC3 PACKAGE (MO-041BA)
Underside View

PAD 1 - Drain
PAD 2 - N/C
PAD 3 - Source
PAD 4 - Gate

FEATURES

- B_{VDSS} =-60V
- I_D = -2.5A
- $R_{DS(ON)}$ = 0.3Ω
- Hermetic Surface Mount Package
- Screening Option Available

The SML2955CSM4 is a very low on state resistance P-Channel enhancement mode mosfet in a Ceramic Surface Mount package designed for high rel applications:

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise stated)

V_{DS}	Drain – Source Voltage		-60V
V_{GS}	Gate – Source Voltage		±20V
I_D	Continuous Drain Current	@T_A = 25°C	-2.5A
I_{DM}	Pulsed Drain Current [1]		-15A
P_D	Power Dissipation	@T_A = 25°C	0.8W
		@T_A = 100°C	0.32W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		156°C/W
T_{STG} , T_J	Maximum Junction and Storage Temperature Range		-55 to +150°C

NOTE:
1) Repetitive Rating: Pulse Width limited by maximum junction temperature.

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Issue 1

SEME LAB

SML2955CSM4

ELECTRICAL RATINGS (T_A = 25°C unless otherwise stated)

	Characteristic	Test Conditions		Min.	Typ.	Max.	Unit
	STATIC CHARACTERISTICS						
$V_{(BR)DSS}$	Drain – Source Breakdown Voltage	V_{GS} = 0V	I_D = -250µA	-60			V
$V_{GS(TH)}$	Gate Threshold Voltage[1]	V_{DS} = V_{GS}	I_D = -250µA	-2.0	-2.6	-4.0	
I_{GSS}	Gate – Source Leakage Current	V_{GS} = ±20V	V_{GS} = 0V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -60V	V_{GS} = 0V			-10	µA
$I_{D(ON)}$	On State Drain Current [1]	V_{DS} = -5.0V	V_{GS} = -10V	-12			A
$R_{DS(ON)}$	Drain Source On-State Resistance [1]	I_D = -2.0A	V_{GS} = -4.5V			0.55	Ω
		I_D = -2.5A	V_{GS} = -10V			0.35	
			T_J = 125°C			0.55	
g_{fs}	Forward Transconductance [1]	V_{GS} = -10V	I_D = -2.5A		5.5		S
V_{SD}	Diode Forward Voltage[1]	V_{GS} = 0V	I_D = -2.5A		-0.8	-1.2	V
	DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{DS} = -30V V_{GS} = 0V	f = 1.0MHz		601		pF
C_{oss}	Output capacitance				85		
C_{rss}	Reverse transfer capacitance				35		
	SWITCHING CHARACTERISTICS						
Q_g	Total Gate Charge	V_{DS} = -30V V_{GS} = -10V	I_D = -2.5A		11	15	nC
Q_{gs}	Gate-Source Charge				2.4		
Q_{gd}	Gate-Drain Charge				2.7		
$t_{d(on)}$	Turn–on Delay Time	I_D =-1.0A V_{GS} = -10V	V_{DD} = -30V R_{GEN} = 6Ω		12	21	ns
t_r	Rise Time				10	20	
$t_{d(off)}$	Turn–off Delay Time				19	34	
t_f	Fall Time				6	12	

NOTES:

1) Pulse Test: Pulse Width = 300µs , Duty Cycle ≤ 2%

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